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A Digitally Configurable ASIC for Sensorless Control of a Switched Reluctance Motor

Bekir Djanklich, Sven Korb, Samuel Lotfey, Maximilian Wiendl, Eckhard Hennig

Abstract—**The current paper presents a digitally configurable ASIC for sensorless control of 8/6 switched reluctance motors. Building on a previous implementation [1], the work in this paper provides improved control capabilities. The main improvement is a current controller with a variable hysteresis, which allows the machine to operate over a wider voltage range. In addition, an improved method for determining the initial rotor position is proposed. The integration of a serial interface allows all parameters of the ASIC to be programmed by the user. As a result, the ASIC can be used to control any 8/6 SRM.**

Index Terms—**Sensorless control, switched reluctance motor, current control, application-specific integrated circuit (ASIC)**

I. INTRODUCTION

Switched reluctance motors (SRMs) work without permanent magnets. The resulting cost advantage can be increased even further by not relying on a position sensor to control the machine.

A suitable sensorless control method has been developed in [2]. The main idea is to energize two phases of the motor simultaneously: To build up torque, a high current is fed through the first phase, which is called the *working phase*. Meanwhile, a second phase, called the *sensing phase*, receives a small ripple current which is used to measure its inductance to determine the rotor position. The assignments of working and sensing phases are shifted around periodically to follow the rotor's movement.

Figure 1 visualizes this sensorless method of position detection. The current i_{P3} in the sensing phase (P3, green) is controlled by an on-off controller. While the rotor turns to align with the working phase (P1, red), its alignment with the sensing phase P3 decreases. This causes the inductance L_{P3} of the sensing phase to decrease as well, which leads to reduced rise and fall times of the sensing current i_{P3}.

As a result, the switching frequency of the current controller is increasing, which can be read from the PWM signal d_{P3}. This frequency increase is exploited to detect the alignment of the rotor: once the PWM frequency f_{P3} reaches the programmed threshold value

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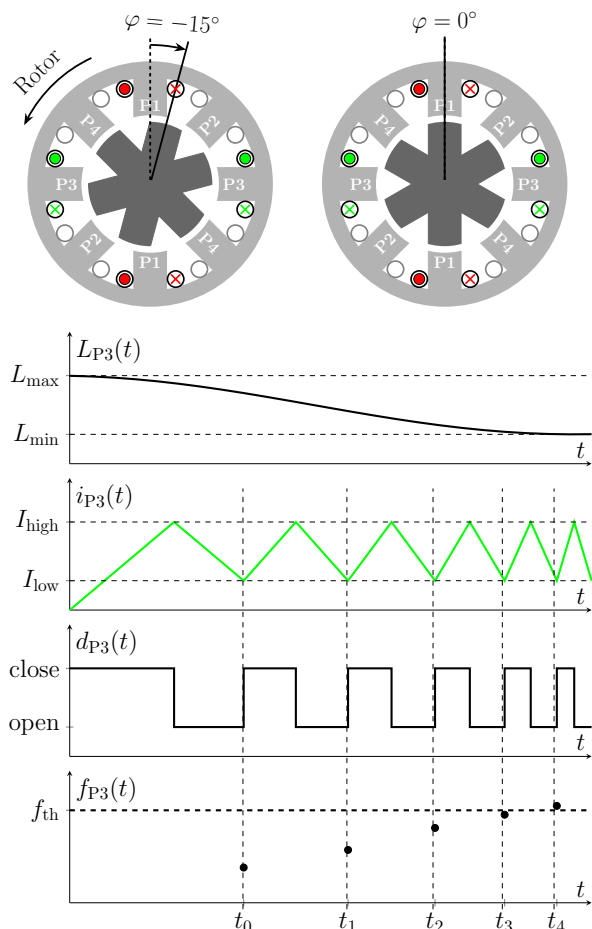

Figure 1. Working principle of the SRM.

f_{th}, the rotor is assumed to be aligned with the working phase, and the working and sensing phases are switched forward one position.

By shortening the time between switching cycles, the granularity of the frequency measurement is increased and the rotor's position can be detected more accurately. Consequently, higher frequencies of the current controller enable more precise phase switches, allowing the motor to turn more smoothly.

Figure 2 shows the circuitry used to control one motor phase, where R_P is the phase resistance and L_P is the phase inductance. The current i_P is fed into the coil by switching the two MOSFETs T_1 and T_2 simultaneously.
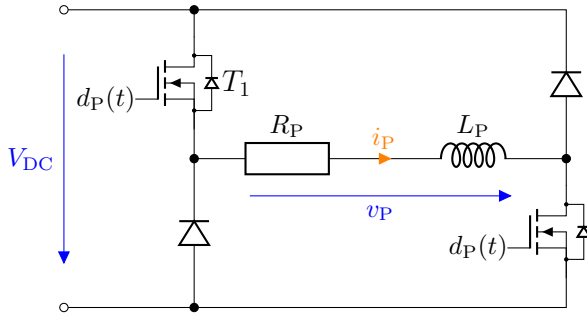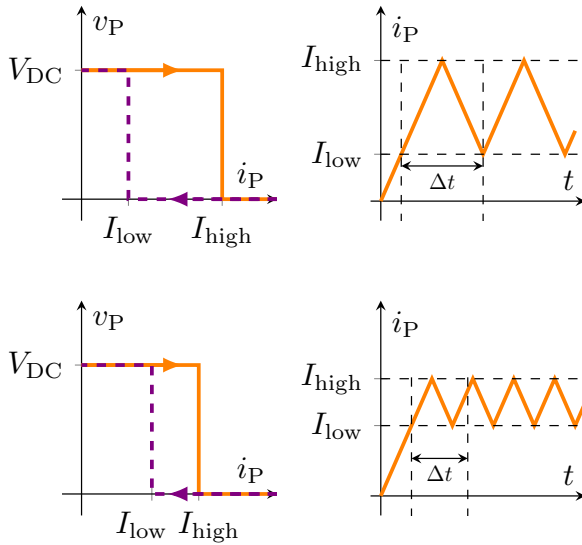
Figure 2. Asymmetric half-bridge topology.

Figure 3. Influence of current hysteresis on the switching frequency of the current controller.
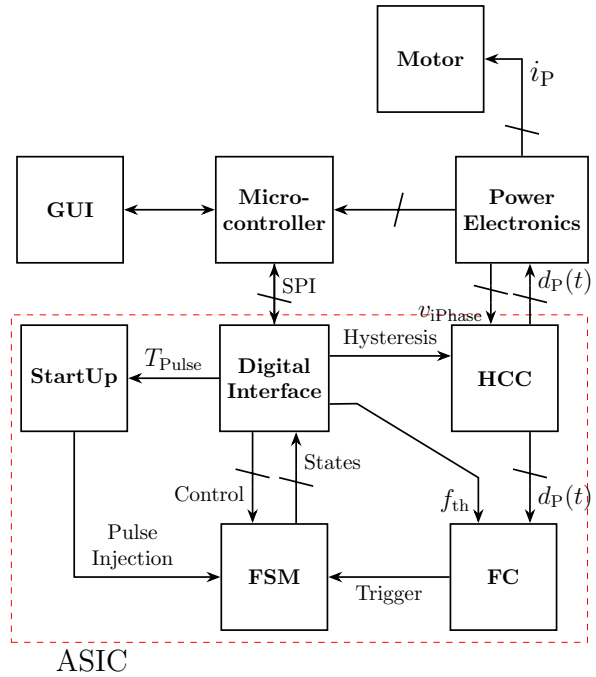

Figure 4. System block diagram.

A further improvement compared to the previous work is the addition of a digital serial interface for configuration and control purposes. It facilitates a fast and automated commissioning process through a large number of configuration parameters.

II. IMPLEMENTATION

A. System Architecture

Figure 4 shows a block diagram of the system.

B. Finite State Machine (FSM)

The FSM is the digital logic that controls if a phase is idling, sensing or working, depending on internal signals and external configuration parameters.

C. StartUp

Since the phase inductances depend on the rotor's orientation, applying consecutive voltage pulses to all phases will cause different currents according to $u = L \cdot \frac{\mathrm{d}i}{\mathrm{d}t}$. By measuring and comparing the occurring phase currents, the rotor's orientation can be determined. This approach, called *Pulse Injection*, was previously used in [3].

Figure 5 shows the improved method that was implemented for the current paper. By applying the voltage pulse to all motor phases simultaneously, instead of consecutively, the time needed for position detection is reduced.

In the example shown, the yellow current rises the least in response to the voltage pulse applied during the Pulse Injection process. Therefore, the yellow inductance (L_{P2}) is the highest, indicating that the yellow
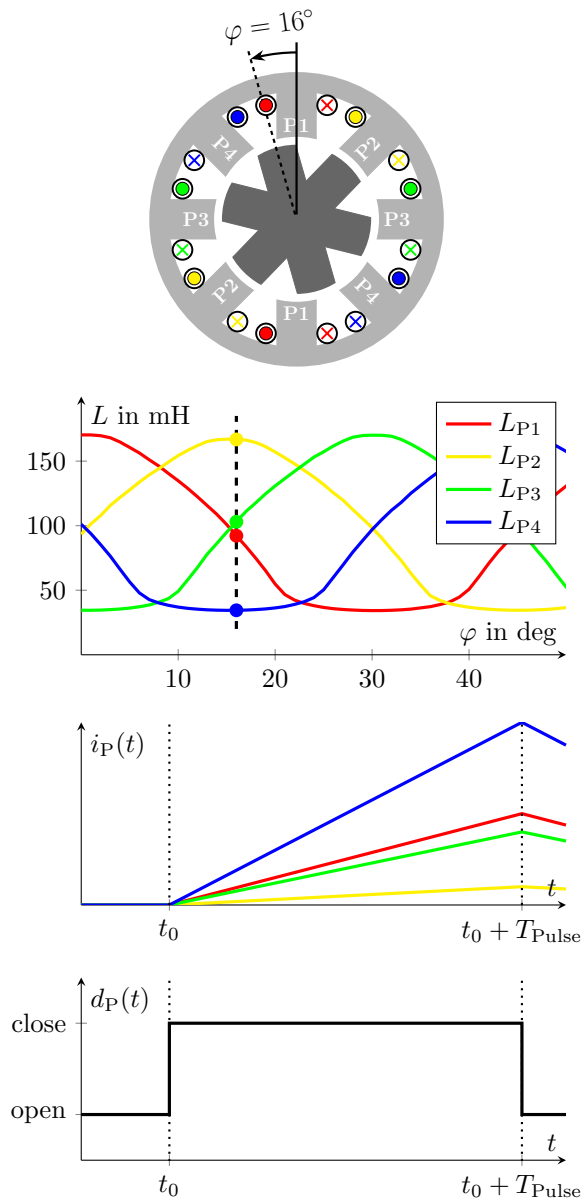
The ASIC developed in the prior work [1] used a current controller with fixed hysteresis. This resulted in low positional resolution in certain working points, causing poorly timed phase switches.

Figure 3 demonstrates how a reduction in hysteresis width increases the current controller's switching frequency, allowing a more accurate measurement of the rotor's position. switching cycles. The work at hand aims to utilize this principle to obtain improved rotational control by implementing a current controller with configureable hysteresis.

With the previous method for sensorless SRM control, it is not possible to determine the initial rotor position before start-up. In the prior work [1], the rotor was moved into a defined starting position by energizing a single phase. During this alignment process, the direction of rotation was not defined. Furthermore, the machine's rotation had to be stopped to perform the alignment process. For the work at hand, a sensorless method for determining the rotor position at standstill was developed and implemented in the ASIC. The new method allows a smooth start-up to be performed even while the machine is still turning.

Figure 5. Pulse injection process.

Figure 6. Structure of the digital interface.

phase (P2) is the most aligned. This information is passed on to the FSM, which uses it to select the correct initial state. Depending on the direction of rotation, either P1 or P3 will be powered next.

D. Digital Interface

The ASIC is equipped with a SPI interface based on [4]. The interface provides 18 registers with 8 bits each, and can be used to read and write configuration and measurement data.

Some 10-bit signals had to be split up into two 8-bit registers, which created the need to read or write multiple registers simultaneously. This requirement is fulfilled through an intermediary buffer memory.
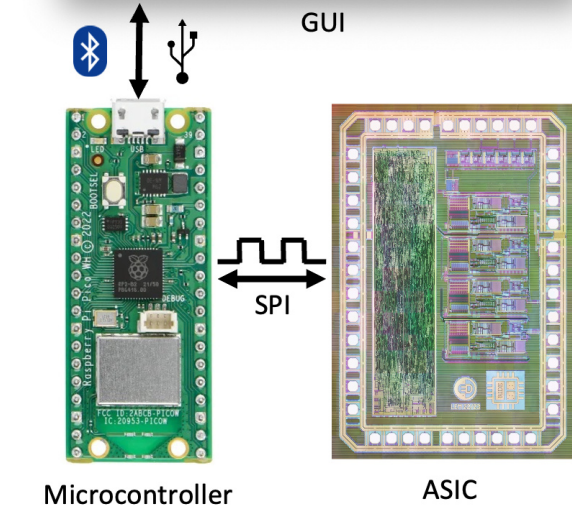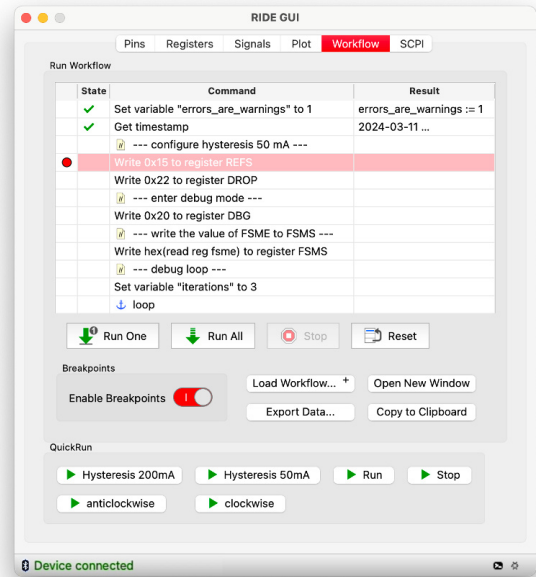
A microcontroller is used to make the functions of the ASIC's SPI interface available via USB or Bluetooth.

User interaction takes place through a custom graphical user interface (GUI), which provides a number of measurement automation, control and data visualization functions. A back-to-back overview of the digital interface is pictured in Figure 6.

E. Hysteresis Current Controller (HCC)

The circuit topology of the HCC, as shown in Figure 7, is the result of rapid prototyping with a focus on using standard library components, instead of a full-custom solution. A configurable hysteresis is implemented through a switched adjustable current sink: When S_5 is switched on, a voltage drop V_{R1} occurs across R_1. The magnitude of the voltage drop depends on the amount of current $n \cdot I_0$ sunk by the
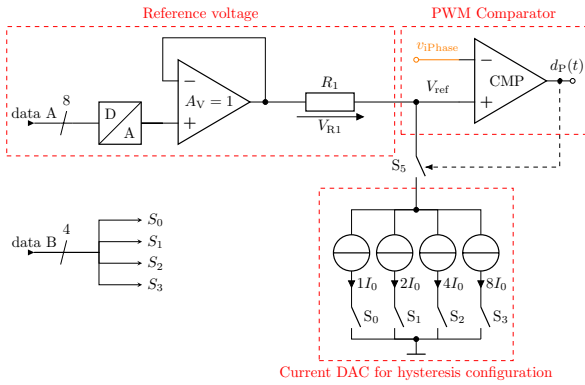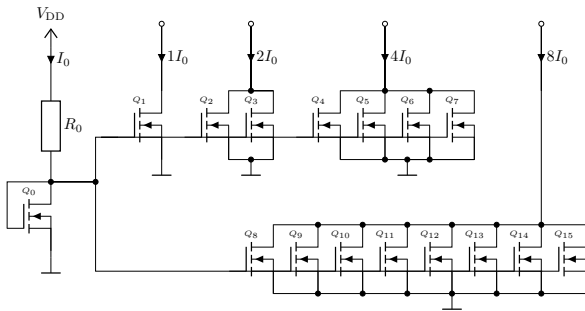
Figure 7. HCC block diagram for one phase.

Figure 8. Current mirror circuit
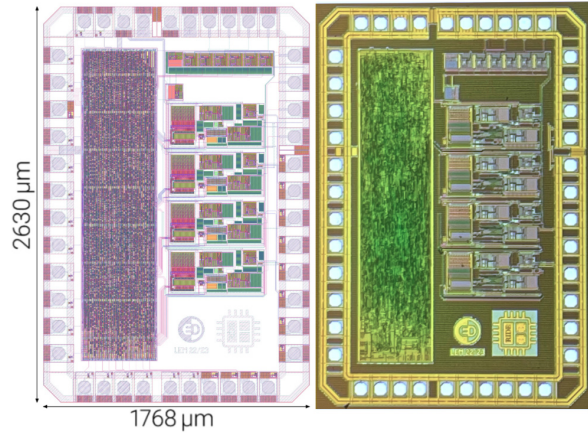

Figure 9. ASIC layout design (left) in comparison to a microscope image of the manufactured die (right).

Figure 10. Smart power electronics system

current DAC. By setting S_1 through S_4 with a 4-bit word *data B*, any multiple of I_0 can be sunk up to a maximum of $15 \cdot I_0$. An 8-bit word *data A* is used to define the reference voltage.

Using this circuit topology, a variable hysteresis of $10\,\mathrm{mV}$ to $150\,\mathrm{mV}$ around a reference point between $0\,\mathrm{V}$ and $3.3\,\mathrm{V}$ can be configured. PWM control signals for each phase's asymmetric half-bridge are generated by comparing the output voltage v_{iPhase} of the phase's current sensor to V_{ref}.

To improve accuracy, the current sinks consist of unit transistors in a current mirror topology, as shown in Figure 8. In the layout, the transistors were matched using the common-centroid method.

F. Frequency Comparator (FC)

The FC measures the switching frequency of the HCC using a digital counter. Once the frequency surpasses a configurable threshold f_{th} (see Figure 1), a trigger signal is sent to the FSM.

G. ASIC Layout

Figure 9 shows the resulting ASIC layout. It is divided into a digital part on the left and an analog part on the right half, which contains the StartUp block at the top and the four HCC instances in the center. The ASIC is surrounded by an ESD frame with pads. It was designed and manufactured using $350\,\mathrm{nm}$ technology with three metal layers.
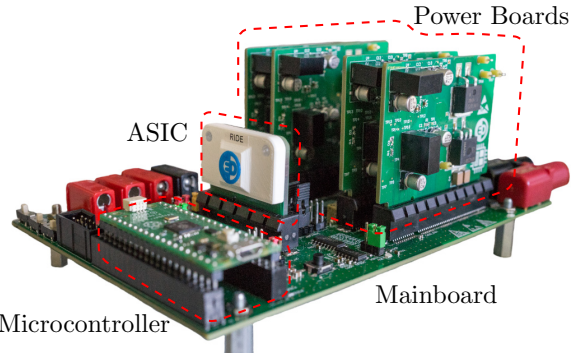
III. Commissioning

For commissioning, the ASIC is placed in the smart power electronics system shown in Figure 10. The ASIC - directly bonded onto an adapter PCB - is plugged into the Mainboard together with four Power Boards. The Mainboard is directly connected to the SRM. Each Power Board contains one asymmetric half-bridge circuit to control the current in one motor phase. This modular design makes it easier to replace components should the ASIC or a Power Board become damaged.

To test the StartUp functionality, the initial rotor position is set to $30°$ as shown in Figure 12. In this position, the inductance in P3 is the highest because it is aligned with a rotor tooth, whereas the inductance in P1 is the lowest. The resulting currents during motor start-up can be seen in Figure 11 (color coding as in Figure 12). The measurement is split into three time frames T_1, T_2 and T_3. Figure 13 shows a separate close-up of the current curves in T_1. During Pulse Injection, the highest current rise can be observed in P1, while the lowest occurs in P3, due to the different phase inductances.

The ASIC correctly determines the rotor alignment based on these currents. Once Pulse Injection is fin-
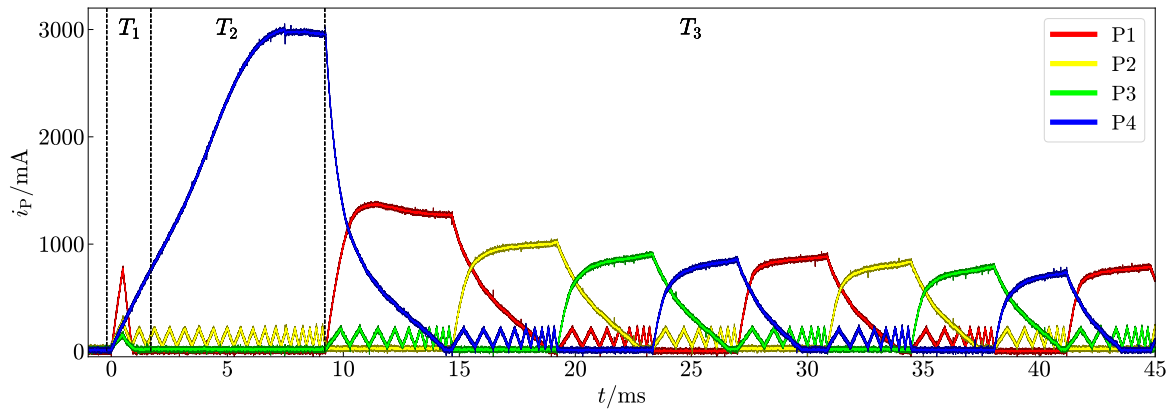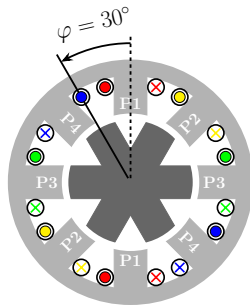
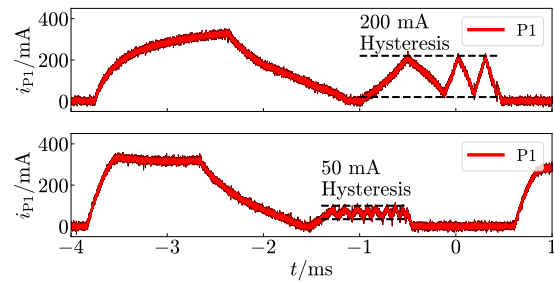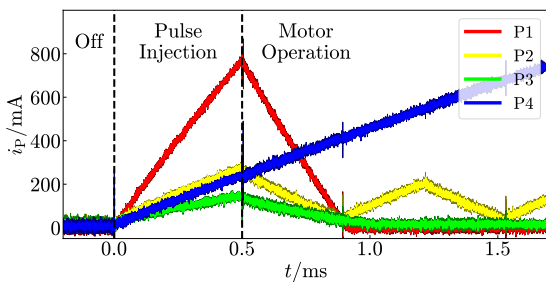Figure 11. Motor phase currents during start-up

Figure 12. Rotor 30° aligned

Figure 14. Hysteresis configuration for higher sensing granularity

Figure 13. Motor phase currents during T_1

Figure 15. Effect of different switching thresholds

ished after $T_\text{Pulse} = 0.5\,\text{ms}$, P4 is selected as working phase and P2 as sensing phase for counterclockwise rotation.

During the time period T_2, a high current is visible in Figure 11. Due to the correlation $M \sim i_\text{P}^2$ [5] between torque M and phase current i_P, the motor draws a high current building up high torque to overcome the moment of inertia.

In time period T_3, the continuous motor operation can be seen. The ASIC energizes the working phases (`W`) and sensing phases (`S`) in the following chronological order:

$$(\texttt{W1},\ \texttt{S3}) \rightarrow (\texttt{W2},\ \texttt{S4}) \rightarrow (\texttt{W3},\ \texttt{S1}) \rightarrow$$
$$(\texttt{W4},\ \texttt{S2}) \rightarrow (\texttt{W1},\ \texttt{S3}) \rightarrow \ldots$$

To test the HCC, the current hysteresis is reduced through the digital interface, increasing the granularity of the frequency measurement as shown in Figure 14. The smaller hysteresis also leads to power loss savings due to smaller currents in the sensing phase.

Next, the threshold frequency f_th is changed from $18.9\,\text{kHz}$ to $9.9\,\text{kHz}$, resulting in earlier phase switching and thus faster rotation as pictured in Figure 15.

Altogether, the measurements prove the correct function of the adjustable hysteresis controller, the StartUp position detection and the serial interface.

IV. Conclusion

The paper at hand introduces improvements to previous ASIC developments for sensorless SRM control which allow the control of any 8/6 SRM. Additionally, the ASIC offers rotor position detection supporting a soft start of the machine, as well as convenient configuration options via an SPI interface.

Acknowledgements

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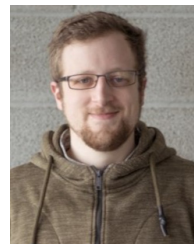
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