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On the Influence of Line Routing and EMC Noise Sources on high-speed Data Transmission and Signal Integrity

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***Abstract*—The aim of this work was to investigate the effect of routing on signal transmission on printed circuit boards in the frequency range of up to 16 GT/s. For this purpose, various boards with different attributes were designed, manufactured and evaluated. In particular, the effects of single and multiple vias, X-vias, microstrip lines, and plane coupling on data transfer were analyzed. Moreover, the effect of interfering signals on the maximum data rate was investigated. For our investigations we use Peripheral Component Interconnect Express, a well-known and frequently used high-speed serial computer expansion bus standard. The examinations include simple benchmarks with regard to the effective data throughput as well as measurement of the signal integrity with an oscilloscope. In total, the eye pattern during signal transmission was measured on ten boards with respect to eye width and eye height. Our results show that modern signal transmission technologies are very mature and robust, and that routing has a surprisingly small influence. Nevertheless, the goal in PCB design should still be a high quality layout, taking best practice routing rules into account.**

***Index Terms*—Printed Circuit Boards, Signal Routing, Data Transmission, Signal Integrity, Interference, Vias, Microstrips, Plane Coupling, Noise, Eye Pattern, PCIe**

I. Introduction

In the automotive industry, analog and power but also high-performance components are widely used to evaluate and process incoming data from sensors like cameras, radar, and lidar. This generates extremely large amounts of data for which very powerful hardware is required. For processing, the data is forwarded to servers via various interfaces on the internet and stored on local SSD hard drives. Due to the high data throughput required for processing data in deep neural networks, corresponding powerful interfaces are needed. Many devices currently rely on the use of Peripheral Component Interconnect Express (PCIe) Gen 4 [1], a serial interface that can also be extended in parallel from an architectural point of view. The individual serial connections are called lanes and work independently of each other. A lane consists of a differential line pair. The gross data throughput of such a lane is up to $16\,\mathrm{GT/s}$, that is, 16 billion bits transmitted in one second. This results in an effective data throughput of roughly $1.8\,\mathrm{GB/s}$. Since one piece of information is transmitted with each clock edge, the effective frequency is $8\,\mathrm{GHz}$. Therefore, the system can only be examined in consideration of line theory, and the laws related to waves apply [2]. Furthermore, this results in various requirements that apply to the development of suitable printed circuit boards (PCBs). Wave properties must also be taken into account in terms of measurement technology, since any measurement influences the signal to be measured [3]. Moreover, the transmission of ideally rectangular, digital signals results in various harmonics. These are subject to strong damping, for example, in the case of impedance jumps. The measurement difficulty then is that the harmonics must also be measured correctly in order to represent the signal correctly. This requires a measurement technique with very high time resolution (sample rate), and measurement adapters and cables that do not attenuate the signal too strongly [4]. In the following, the aim is to understand and describe the physical conditions. We will derive corresponding rules, based on the specifications, for physical implementation, which will then be examined in various specific cases of use.

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II. Fundamentals

This Chapter covers the relevant basics that are required for the analysis and measurements of this work. In Chapter II-A, transmission lines are examined with a focus on the telegraph equation (1). Next, the properties in the very high frequency range are considered, and finally the model is extended to a three-wire system, as it is used in practice for differential (balanced) lines on PCBs. Chapter II-B then addresses the problems and challenges in applications. Assumptions regarding the development of PCBs will be examined and discussed in Chapter II-C.

A. Transmission Line

1) Real Lines and Wave Impedance: In theory, a wire establishes an electrical connection between two points. For most simple electrical circuits, this model is quite sufficient. To complete an electric circuit, a

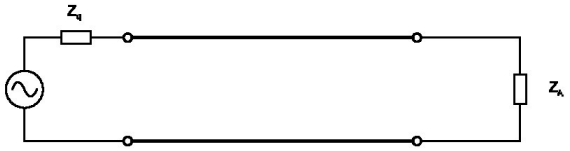


Figure 1. Ideal electric connection.

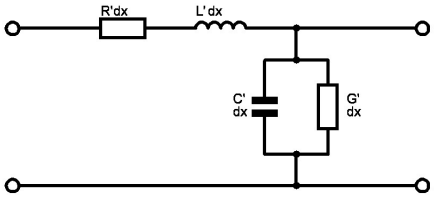


Figure 2. Equivalent circuit diagram of a real line [6].

forward and a return conductor are needed. This is shown in Figure 1.

Now we begin to differentiate between ideal connections and real lines. First, we will look in detail at the line segment shown in bold in Figure 1. It is obvious that a line has an ohmic resistance, comparable to the filament of a light bulb. Accordingly, losses and thus a voltage drop occur on a line. They depend primarily on three factors: The length of the cable, the cross-section of the cable, and the specific conductivity of the material used. Furthermore, the conductance of the insulator between the lines is subject to the same dependencies as the specific line resistance. With a DC application we could end our investigations here, but this is not the case with RF transmission lines.

Figure 2, for example, shows that there is an - admittedly small - capacitor between two lines. Accordingly, a pair of lines has shunt self capacitance which, in addition to the ohmic properties of a conductor, also leads to a change in the signal depending on the frequency. With PCBs, there is no analytical method to determine these. This is due to the geometric shape of the conductor lines [5] [6]. Finally, there is a less descriptive property in this model: The series inductance of a line. To make this tangible, we imagine a line as an unwound coil. The self inductance is not lost in the physical model of a coil either.

In order to keep these different properties manageable for technical applications, wave impedance Z_l is introduced to model the equivalent circuit shown in Figure 2. It is calculated according to the Telegraph Equation (1). The apostrophes illustrate that we are not dealing with discrete components, but with conduction properties.

$$Z_l = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}} \tag{1}$$

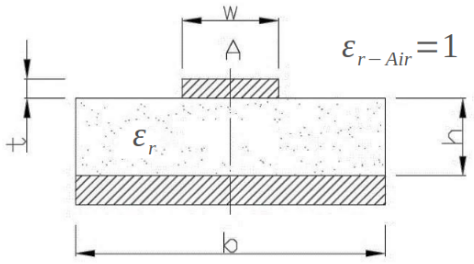


Figure 3. Cross section of a microstrip line [6] [7].

Wave impedance facilitates the calculation of high-frequency signals. Even if the skin effect increases the series resistance as the frequency increases, the real-value series resistances are so small that they are negligible. The same holds for the shunt conductance: At a sufficiently high frequency, it is negligible. Thus, Equation (1) can be simplified as follows:

$$Z_l \approx \sqrt{\frac{L'}{C'}} \tag{2}$$

If the wave impedance changes from one section of the line to another, this leads to reflections. That results in a loss of wave energy and therefore also to an attenuation of the signal. The reflection factor r can be calculated according to Equation (3).

$$r = \frac{Z_{l2} - Z_{l1}}{Z_{l2} + Z_{l1}} \tag{3}$$

2) Transverse Electromagnetic Modes and Waveguide Properties: We will now focus in greater detail on the wave properties. Signals with a sufficiently high frequency only need to be considered on the basis of their wave properties. An ideal, lossless wave that travels only with transverse amplitudes in the direction of propagation is generally called a transverse electromagnetic mode (TEM) or TEM wave in the context of propagation. Thus, a guided, progressive wave is formed between two conductors. In the strict physical sense, such a wave does not exist, since each conductor has losses and therefore the voltage drops by a very small amount. However, this effect is so small that further treatment takes place at an ideal wave. Classic examples of such two-wire lines are parallel lines (twisted pair), coaxial lines and microstrip lines. The latter can be easily and cheaply implemented on PCBs and therefore enjoy very frequent use.

As shown in Figure 3 it is important that the width b of the ground plane is considerably wider than the width w of the microstrip. Furthermore, the height of the trace is described by t and the thickness of the insulator with the dielectric constant ϵ_r by h. However, the entire conductor is not surrounded by a shield as would be the case with a coaxial cable, for example. The electromagnetic field propagates differently

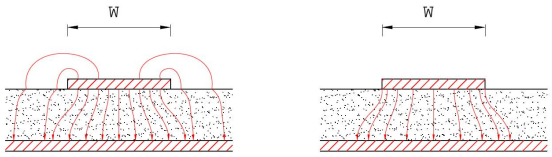


Figure 4. The electric field of the microstrip line at low (left) and high frequencies (right) [6] [7].

depending on the frequency, which also leads to a change in the conductor track impedance. Therefore, it is a great challenge to apply microstrip lines for a wide frequency range [7]. Figure 4 shows that the electromagnetic field does not propagate in a constant dielectric but in a layered dielectric consisting of air and substrate, the dielectric constant values of which differ from each other.

As a result, the behavior is described by an effective dielectric constant $\epsilon_{r,eff}$, which can be calculated according to [7] [2] [3] [8]:

$$\epsilon_{r,eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \cdot \left(\frac{1}{\sqrt{1 + 12(h/w)}}\right) \quad (4)$$

There are three main factors that characterize the impedance Z_l of a line: First, the effective dielectric constant $\epsilon_{r,eff}$ calculated with Equation (4). Second, the width of the microstrip w and third, the height of the dielectric h. Depending on the ratio between width and height, the dependencies as stated in Equation (5) arise [7].

$$Z_l = \begin{cases} \dfrac{Z_0}{2\Pi\sqrt{\epsilon_{r,eff}}} \ln\left(8\frac{h}{w} + \frac{w}{4h}\right) & \text{when } \frac{h}{w} \leq 1 \\ \dfrac{Z_0}{\sqrt{\epsilon_{r,eff}}[\frac{w}{h} + 1.393 + 0.667\ln(\frac{w}{h} + 1.444)]} & \text{when } \frac{h}{w} \geq 1 \end{cases} \quad (5)$$

However, it should be noted that this is not an analytical calculation of the impedance but only an approximation. Influencing factors arising from manufacturing can only be taken into account to a limited extent. For example, manufacturing techniques may result in the microstrip no longer being rectangular but being given a V-shape, for example, due to underetching. Wave impedance can be tested and measured using a time domain reflectometer (TDR). Here, an edge of known amplitude at the open end of the source is propagated down the line to be tested. Since the wave impedance at the feed is known, the characteristic impedance Z_l can be determined from the reflected signal at the open end. Here v is the injected signal, a the reflected signal and Z_s the impedance of the source [9].

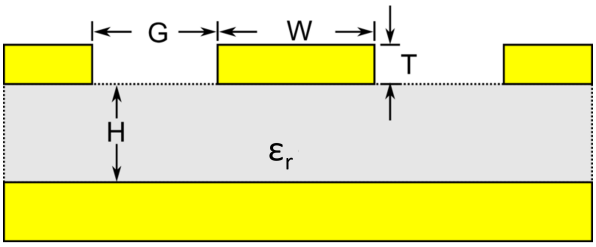


Figure 5. Cross-section of a coplanar waveguide [10] [7].

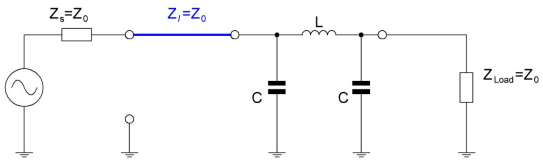


Figure 6. Asymmetric single ended transmission line [6].

$$Z_l = Z_s \frac{a/v}{1 - a/v} \quad (6)$$

3) Differential Signaling: For applications requiring high frequency stability, coplanar waveguides can be used. These are transmission lines having a ground plane on the same layer as the signal line. The signal line is located between the surrounding ground planes and separated by a gap. A ground plane is also located under the substrate and a thin topcoat is applied over the circuit. Such a line is shown in Figure 5. The biggest benefit is good suppression of crosstalk between several microstrip lines [9] [7].

The speed of wave propagation ϑ_p of a TEM wave depends on the effective dielectric constant $\epsilon_{r,eff}$ of the transmitting medium and can be calculated as follows [7]:

$$\vartheta_p = \frac{c_0}{\sqrt{\epsilon_{r,eff}}} \quad (7)$$

We will now consider the previously introduced line as an unbalanced single ended (SE) system, also called a two-wire system. This is because one line always has the ground function and circuits are therefore designed asymmetrically. For example, an unbalanced low-pass filter is shown schematically in Figure 6.

This design is very popular in applications because it is easy to calculate. However, it is subject to some disadvantages, namely that interference has an unbalanced effect on the signal. Therefore, digital applications require signal levels with a sufficiently high amplitude so that the signal can be correctly detected at the line end. Due to the capacitive behavior of a line, a sufficiently strong driver is therefore required. This leads to many other issues; for example, the currents for high frequencies, which are equivalent to high data rates, are associated with high magnetic field strengths,

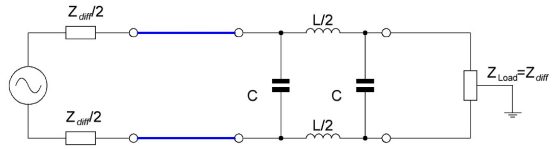


Figure 7. Symmetric three wire differential signaling transmission line [6].

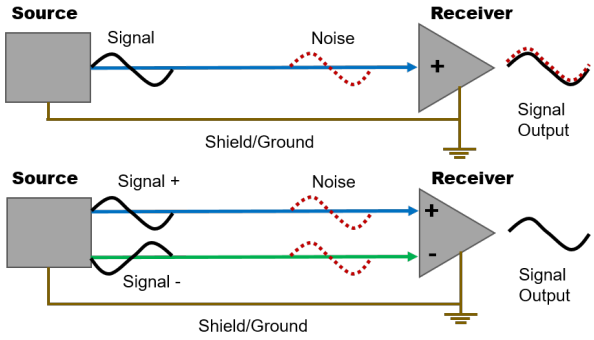


Figure 8. Noise on single ended vs. differential transmission line [11].

which have a disruptive effect on neighboring circuit parts. In addition, corresponding powerful driver transistors need, correspondingly, more space on the wafer and lead to high heat dissipation. All these problems are avoided by introducing a symmetrical three-wire system. The same filter as in Figure 6 is shown in Figure 7 using a symmetrical three-wire system. The contact in the center of the load resistor represents the reference to the ground potential.

What at first glance looks like a considerably greater amount of extra effort offers several advantages. As can be seen in Figure 8, coupled interference has the same effect on both lines.

While the signal at the top of Figure 8 is superimposed by the noise at the output, this effect disappears in the line shown in the lower part of Figure 8 after both transmitted signals have been subtracted from each other. This enables a reduction in the required voltage swing at which the signal can still correctly be recognized at the receiver. Since the transmitted signals are equal but have opposite polarity, the driver only needs an additional inverter, which does not impose significant extra effort on a chip. Due to the symmetrical design, injected currents induce a counter-current on the complementary line, which again reduces susceptibility to errors as well as emitted radiation. Thus, the cost is only a single additional line, with the condition that both lines have the same length, are close together, and have the same dimensions so that the wave impedances match and no reflections occur [9] [6].

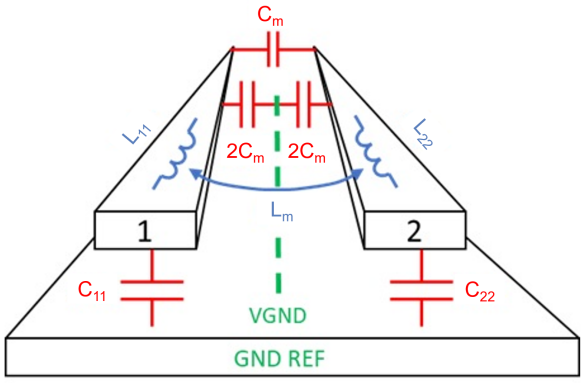


Figure 9. Pair of microstrip traces showing self-loop inductance (L_{11}, L_{22}), self-capacitance (C_{11}, C_{22}) mutual capacitance (C_m) and mutual inductance (L_m) when line 1 and line 2 are driven differentially [12].

The physical properties as well as the calculation of these are similar to the single ended (SE) line. However, the electromagnetic fields interact with each other due to coupling, which can be described by introducing a virtual ground (VGND). This is illustrated schematically in Figure 9.

The special thing about determining the impedance is that two modes, even and odd, can propagate on a differential pair of lines. The odd mode, in which the signal on both lines has an inverted polarity, is preferred. With the even mode, this is not inverted, which is why the electromagnetic fields interact differently with each other and therefore also have an effect on the differential wave impedance. This results in a new parameter for the SE line, named Z_{odd}. With $L_S = L_{11} = L_{22}$ and $C_S = C_{11} = C_{22}$ the impedance can be calculated according to Equation (8) [12] and Equation (9) [13].

$$Z_{odd} = \sqrt{\frac{L_S - L_M}{(C_S + 2C_M)}} \tag{8}$$

$$Z_{diff} = 2 \cdot Z_{odd} \tag{9}$$

As with the microstrip line, there is also an equation to approximate the differential wave impedance. It is based on the dimensions of the line as shown in Figure 10 and is calculated according to Equation (10) [13].

$$Z_{diff} = \frac{174}{\sqrt{\epsilon_r}} ln\left(\frac{5.98 \cdot h}{0.8 \cdot w + t}\right) \cdot (1 - 0.48 \cdot e^{(-0.96\frac{d}{h})}) \tag{10}$$

B. PCB Construction and Connection Technology

Like a sandwich, a PCB consists of different layers. Conductive layers, where the signal routing is located, are pressed between electrical insulating layers. This way, components that are physically separated from each other can be connected on conductive layers.

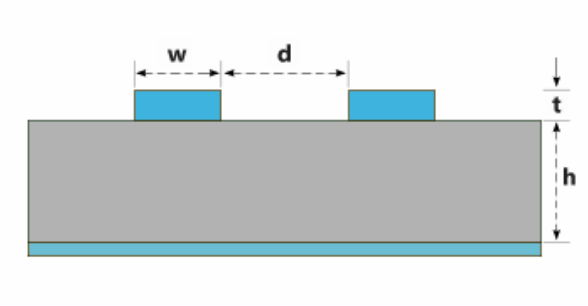


Figure 10. Cross section of a differential microstrip [13].

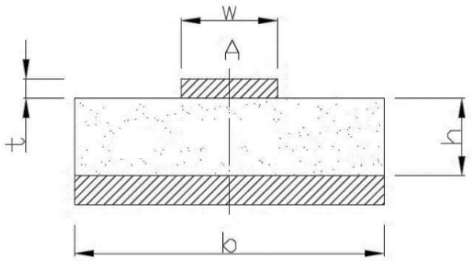


Figure 11. Microvia compared to Plated Through-Hole (PTH) [14].

It makes sense to take a systematic approach here. For example, with two-layer PCBs, it is common to lay only vertical connections on one layer and only horizontal connections on the other. Even components whose lines cross in the circuit diagram can thus be connected to each other. With more complex layer structures, it is possible to bring more structure into the design as well as to implement more technology in physical form.

A typical example is the connection of microcontroller chips. It is common to bring their pins quite close together, which has the distinct advantage of reduced hardware dimensions but requires more complexity in terms of design. Therefore, multi-layer PCBs with more than 4 layers use the inner layers for routing Power Delivery Networks (PDN) and ground. The use of the central ground layer improves signal integrity. Due to the separation in terms of conductivity, the electric field cannot crosstalk from the two outer layers and thus influence the signal path on the opposite line. This is particularly advantageous for signals that operate at high data rates. Connections between different layers are made by drilling a hole which is then plated with copper through a galvanization process. This simplest type is called Plated Through Hole (PTH) shown in Figure 11 on the right. In another process, a laser is used to burn a hole through the outermost prepreg layer, an insulating composite made of a glass fiber mat soaked in synthetic resin, and then electroplated. Such a structure is called microvia and shown in Figure 11 on the left.

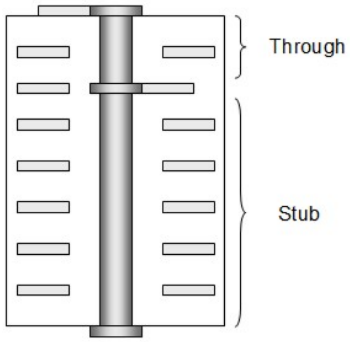


Figure 12. Via stub [17].

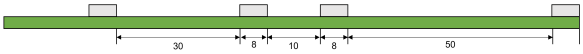


Figure 13. 3W rule (left) and 5W rule (right) horizontal on a PCB.

Microvias are more expensive compared to standard vias but offer two advantages: First, they save space, and second, they improve signal integrity for higher frequency signals. This is due to the absence of a stub as shown in Figure 12, which is a loose wire end that causes reflections that impair signal integrity.

Considering signal integrity means that the layout and routing of a signal line from the transmitter to the receiver are implemented in such a way that data transmission quality is maintained. At a data rate of 16 GT/s, the length of the via stub is in the range of 10% of the wavelength, and an impact on the signal is therefore to be expected. With through-hole vias, integrity can be improved further by removing unconnected residual rings on the intermediate layers and setting up a larger area without copper around the pad of the vias, the so-called anti-pad. However, it is not only the vias that have an impact on signal integrity but also the routing. The higher the applied frequency, the more likely it is that kinks in the line should be avoided. Instead, directional changes are accomplished through the curved course of the conductor paths. To avoid crosstalk on neighboring lines, the distance from neighboring lines can be increased. Usually, the $5W$ rule applies, where the next line should be at least five times the conductor width W away. However, it is even better to surround the line with a ground plane that is well connected to the other ground layers. The $3W$ rule, which means a distance between the line and the ground plane of three times the width of the conductor, is sufficient here [1].

When developing a PCB, it may be necessary to route a PDN on a layer neighboring the microstrip line due to space. This is problematic because there is a jump in the wave impedance at this point. This can be compensated by coupling capacitors such as those in Figure 14, which guarantee the correct routing of the return current.

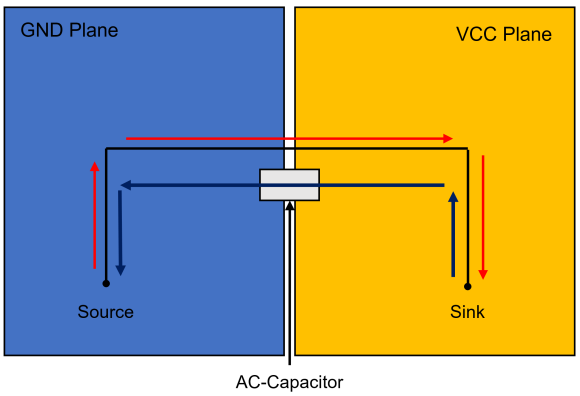


Figure 14. AC-Coupling capacitor.

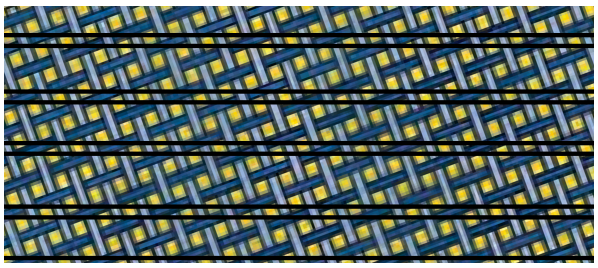


Figure 15. Rotation of the underlaying PCB fiber weave [15].

If a line is routed inside a PCB, it is also called a stripline. This has the advantage that there is even better shielding against interfering signals and better electrical coupling. As described above, the insulating layers are made of a woven glass fiber mat impregnated with epoxy resin. Due to this structure, this material offers no completely homogeneous properties. The glass fiber has a different relative dielectricity to the resin. To avoid any potential problems, either the prepreg can be pressed at a different angle during production or the entire design can be rotated by an angle of 20°, for example, when creating the production data. Figure 15 shows a typical example, where the prepreg is tilted relative to the lines.

C. Peripheral Component Interconnect Express

1) Constraints and Hardware Specifications: The physical properties and requirements discussed above are taken for granted in the specifications for PCIe. A consortium founded by various companies, the PCI-Special Interest Group (PCI-SIG), takes responsibility for publishing complete specifications containing all the necessary information to establish a securely functioning data connection between a host and its peripherals. The characteristics of the PCIe specifications are discussed below.

The PCIe bus is a high-speed bus with point-to-point topology and independently operating serial links. A link is an established data connection implemented on one lane. A lane consists of one differential line pair.

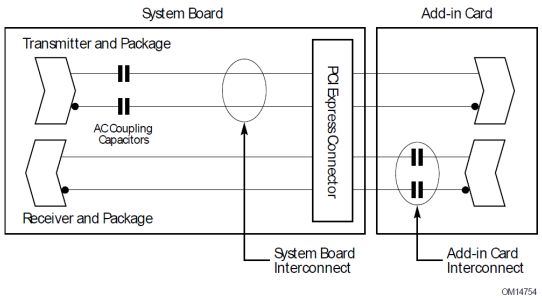


Figure 16. Link definition for two components [16].

The bus width can range from one to typically sixteen lanes. A bus width of 32 lanes is also envisaged but is not yet common in practice. Each lane can perform upstream and downstream data transfer as discussed in Chapter II-A3. The first pair is the sending lane, also called TX (transmit). On this lane the data is sent from the root complex to the endpoint. The latter pair of lines is used to send data from the endpoint to the root complex, which is why it is referred to as RX (receive) from the root complex perspective. Since the frequency is proportional to the applied data rate, which is in the range of Giga Hertz, it is essential to consider the wave characteristics introduced in Chapter II-A. The differential wave impedance used was set to the range of 72.5 Ω to 97 Ω. If there is a mechanical connector between the root complex and the endpoint, it is recommended that the SE impedance for auxiliary signals is in the range of 42.5 Ω or 50 Ω ± 7%. This is because there must not be a ground layer in the area surrounding the contacts, which can lead to crosstalk from the RF signals to the auxiliary signals. In addition, it is recommended that these signals are connected to plug-in cards with a CR element consisting of a capacitor with a capacitance of 1 pF and a resistor of 42.5 Ω or 50 Ω with a tolerance of 2 Ω.

AC coupling capacitors with a capacity of 220 nF are located in the lanes. Since the wave impedance changes at the connection pad, ceramic capacitors of size 0201 are recommended as shown in Figure 16 [1] [16].

The polarity of the differential line pair may be swapped in routing as desired, which simplifies the routing effort and therefore also has a positive effect on signal integrity. However, the difference in length between the individual lines due to routing must not be greater than 0.064 mm. The specifications do not limit the maximum number of vias. Various manufacturers use different numbers in the range of 1 to 6 vias. Via stubs are not permitted, however.

The thickness of plug-in cards is specified as 1.57 mm, with a tolerance of 0.13 mm. The exact dimensions from plug-in area to card edge are given, as well as the height and width for different module sizes. The edge for the insertion area should be milled

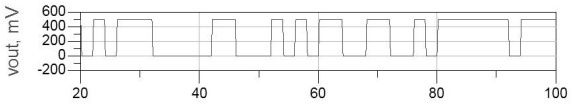


Figure 17. Example of a signal over time [5].

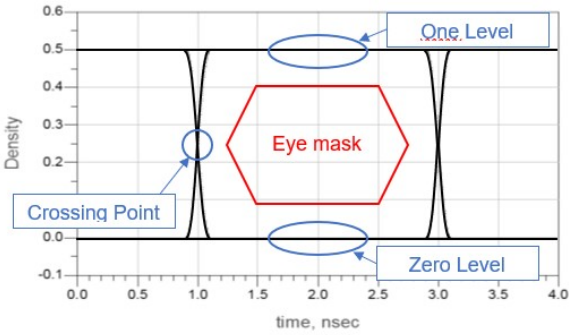


Figure 18. Eye pattern [5] [4].

with a 20° angle to protect board and socket during the insertion process [1] [16].

2) Eye Pattern, Jitter and Bit Error Rate: Figure 17 shows a signal over time.

In order to assess signal integrity, the shortest time unit between two edges is measured. An internal trigger signal is derived from this, and all edges are superimposed on the same point. Later, this time period is used as a unit interval (UI). The result then becomes a signal curve as shown in Figure 18. This representation is commonly referred to as "eye pattern" or "eye diagram".

Signal integrity can now be analyzed based on the eye pattern. The central opening is the reason for the name of this type of representation. The so-called mask is shown in red in the center of Figure 18. This area must remain blank according to the specifications for any signal. Depending on the protocol, the mask may look different. The Bit Error Rate (BER) is a measure of the frequency with which the mask is violated. It is defined as the ratio between the incorrectly transmitted bits and the correctly transmitted bits. Ideally, it is 0 or as low as possible. If the error rate becomes higher than 10^{-12}, the link is cancelled and renegotiated. The procedure for this will be presented in the following Chapter II-C3.

Besides the BER, many other parameters can be quickly read from an eye diagram: The eye height is the vertical difference between the zero and one level, also named the vertical eye opening. Ideally, the eye crossing point is exactly 50% of the eye height. The temporal distance between the two crossing points is the eye width. Another important feature is the jitter. This is determined by displaying the spread of the crossings at the crossing point using histograms. The rise time is the time it takes for the signal to rise from 20% to 80% signal level, while the fall time is exactly the opposite.

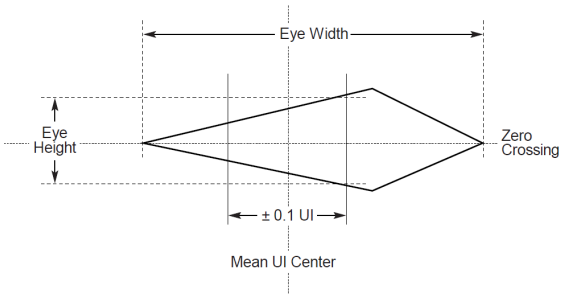


Figure 19. Minimal requirements at the receiver, illustrated in the mask with eye height and eye width [1].

Table I
16.0 GT/S CHANNEL TOLERANCING EYE MASK VALUES FOR [1].

Symbol	Parameter	Value	Units
UI	Unit Interval	62.48125 (min) 62.51875 (max)	ps
$V_{RX-CH-EH-16G}$	Eye height	15 (min)	mVPP
$T_{RX-CH-EH-16G}$	Eye width at zero crossing	0.3 (min)	UI
$T_{RX-DS-OFFSET-16G}$	Peak eye height offset from UI center	± 0.1	UI

3) Link Initialization and Training: According to the PCIe specifications, the binary states 1 and 0 are represented by voltage values. None of them correspond to 0V, which is why we speak of non-return-to-zero (NRZ). To ensure that only the AC mode exists during data transmission, the 8b10b coding is used for PCIe Gen 1 and 2. Here, no bytes but only 8 bit symbols are transmitted, with a maximum parity difference of ±2. The other 2 bits are used to compensate the odd parity. Therefore, 20% of the transmitted data contains no information but overhead bits. In contrast to this, PCIe generations 3 and 4 use 128b/130b coding. Here the sequence starts with a 0-1 toggle and is followed by a 128 bit long data packet. It is assumed that the signal no longer has a DC component on time average. For the receiver, the PCI-SIG provides a mask for the eye diagram in a diamond shape as shown in Figure 19. The most important characteristic limit values can be found in Figure II-C3.

Due to the characteristic properties of a trace, edges are strongly attenuated by the inductive behavior. This can be compensated by applying the following three countermeasures as illustrated in Figure 20.

First, de-emphasis at the beginning of an edge alternation is achieved by applying a higher signal level for a short period of time. Second, if a signal state is present for a longer period of time, the signal level

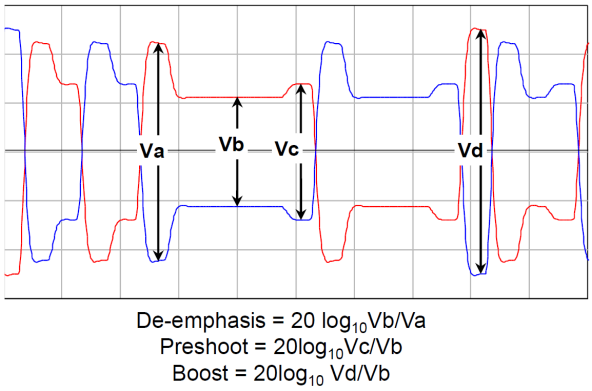


Figure 20. Definition of Tx voltage levels and equalization ratios [1].

can be slightly increased by a preshoot before the state transitions. This increases the steepness of the falling edge. Third, a boost is applied especially for 010 or 101 state changes. For link training, eleven different presets of these individual equalization ratios are specified.

When setting up a link, the root complex and the endpoint synchronize via the reference clock after the power supply is applied to all components involved. In the next step, the receiver starts with the RX detect to check on which input a line is located, then the devices, individually on each lane, start sending serial data at a rate of 2.5 GT/s. This is the absolute minimum speed at which the devices can send data according to the original PCIe Gen 1 specifications that must be supported by any PCIe device.

After the physical connection has been recognized, polling begins. Training sequences at PCIe Gen 1 speed are sent from the root complex to the endpoint. Meanwhile, the receiver tries to synchronize itself with the known sequences. This is performed until the bits are correctly recognized first, then the endpoint tries to decode the transmitted 1-0-bit symbols. The last step is to compensate for the different line lengths of the individual lanes. Once this is complete, the system is in L0 state, which means normal mode.

Link training for PCIe Gen 2 is the same as for GEN 1, except that different symbols are sent during polling.

To establish a Gen 3 or Gen 4 link, an L0 state link must already exist. Starting with this, the equalization phase begins. Here, training sequences with the different presets are sent and the receiver tells the transmitter at which preset the data is best received and again the L0 state is reached. Gen3 L0 state is negotiated first before the negotiation of Gen 4 is started. There is an option to start the training of the equalization connection for a Gen 4 connection directly. However, this only makes sense for embedded systems with known and defined modules.

III. Introduction to the Investigated Hardware

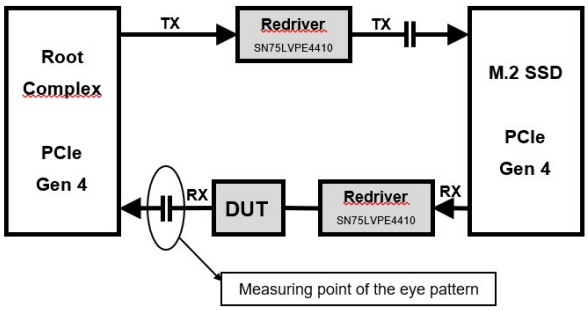


Figure 21. Flow chart of the test setup.

A. Research Concept

To assess the effects of routing on signal integrity, a system available on the consumer market is used. The root complex consists of a CPU on a mainboard, which meets the required PCIe 4.0 specifications. The endpoint is a compatible peripheral device. We use a latest generation M.2 solid state drive. Various plug-in cards are to be plugged in between to evaluate the effects of signal routing. They will be presented and discussed in greater detail in Figure III-B. In order to keep the impact of the plug-in connections as low as possible, a redriver ensures that the signal is reprocessed. However, this is pure signal amplification without any combinatorial logic. In addition, this component increases comparability among the evaluated PCBs. On the RX line, namely the line on which data is transferred from the hard disk to the root complex, different types of line routing implemented on the plug-in cards are to be investigated. In Figure 21, this is the device under test (DUT).

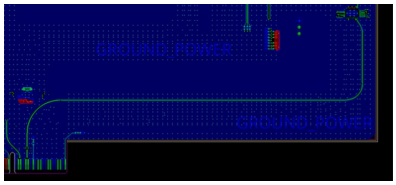
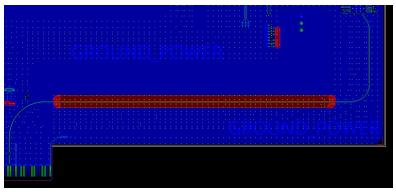
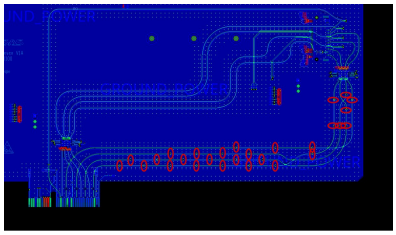
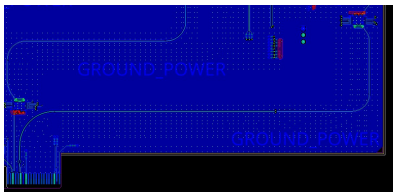
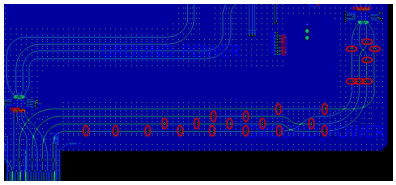
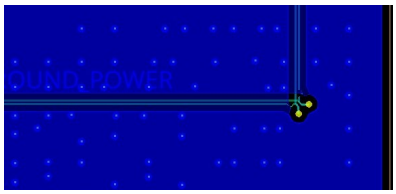
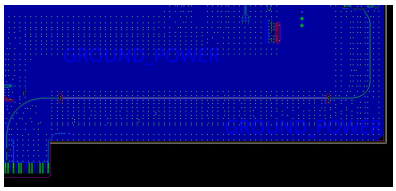
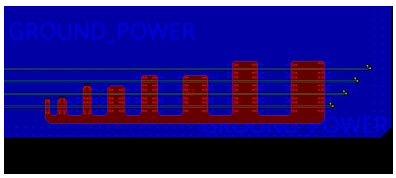
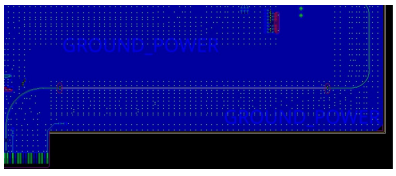
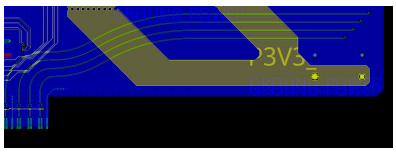
In theory, a link will work if all the rules of the PCIe specifications are met. To evaluate the effect of signal routing, the requirements of the specifications were systematically violated by implementing various design alternatives. This means that, as far as possible, one rule was broken for each board examined. The subject of the investigation was initially subject to a simple pass or fail. Data transmission performance is then examined in greater detail. For this purpose, there is a tool "performance test" that is already included in the operating system used, Linux Ubuntu 22. The signal characteristics of the AC coupling capacitors are to be measured and examined with an oscilloscope.

B. Plug-in Cards

For the examinations carried out in this work, a total of ten plug-in cards were developed. Figure 22 and Figure 23 provide an overview of one of these plug-in cards, which is used as reference for further analysis.

The reference plug-in card, as well as the nine other designed and investigated plug-in cards are contained and described in Figure III-B.

Table II
OVERVIEW ON THE 10 DESIGNED AND EVALUATED PLUG-IN CARDS.

Board name	Test subject	Board name	Test subject
No via	 This board is the reference for all following investigations. It is a PCB with exactly one lane on which all the rules of the specifications are observed.	Plane Coupling	 The design is the same as the "No via" board, except that part of the trace is routed on another plane. In this region, this transmission line is not coupled to the ground potential. This should have an influence on the wave impedance and lead to reflections. However, it is possible to couple the reference plane to ground power, as shown in Figure 14.
Even via count (x4)	 The effects of vias on the signal path and data throughput are to be tested. For this purpose, 4 (lane 1) to 10 vias (lane 4) per lane are on the board. Via locations are marked in red.	Single via	 The design is the same as the "No via" board, except that a via conducts the signal from the top to the bottom.
Odd via count (x4)	 The effects of vias on the signal path and data throughput are to be tested. For this purpose, 3 (lane 1) to 9 vias (lane 4) per lane are on the board. Via locations are marked in red.	Single X-via	 The design is the same as the "Single via" board, except that the via has a 90° bend.
Micro-stripline	 The design is the same as the "No via" board, except that part of the trace is routed as a stripline on an inner layer. The intermediates have been marked in red.	Plane Coupling V2	 This design is a step up from the board "Plane Coupling": The aim is to investigate the effect of multiple uncoupled line segments.
Micro-stripline Microvia	 Just like the board "Microstripline", except that the stubs are eliminated by the use of microvias.	EME	 The effect of an interference source is to be investigated on this board. For this purpose, the lanes are crossed by a PDN on an inner layer through which a high, pulsating current flows.

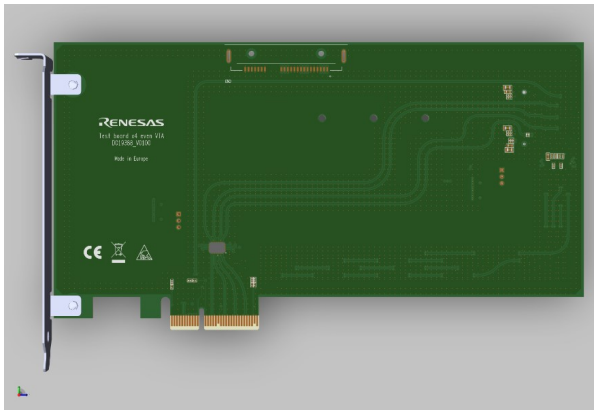


Figure 22. Top view of the reference plug-in card.

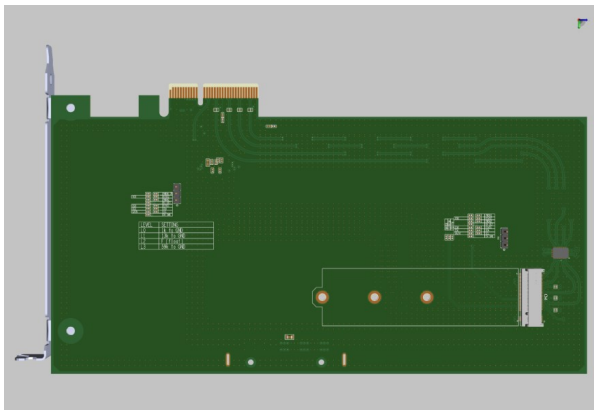


Figure 23. Bottom view of the reference plug-in card.

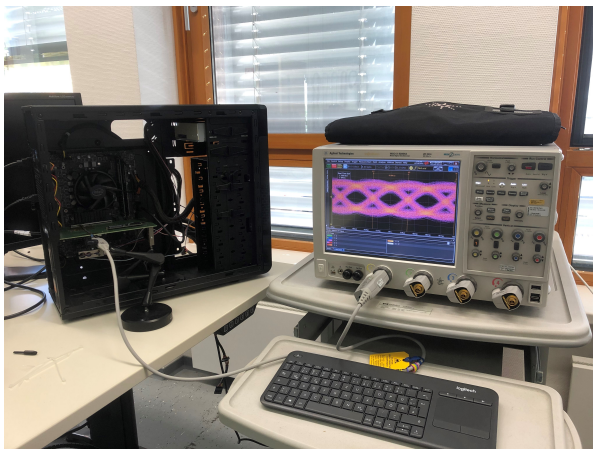


Figure 24. Used oscilloscope with test system.

C. Measurement Setup

The signal integrity is measured with an oscilloscope as shown in Figure 24. This device has a resolution of up to 80 GS/s and is therefore fast enough for a measurement of PCIe Gen 4. An active differential probe is used, which was specially developed for the measurement of Low Voltage Differential Signals (LVDS).

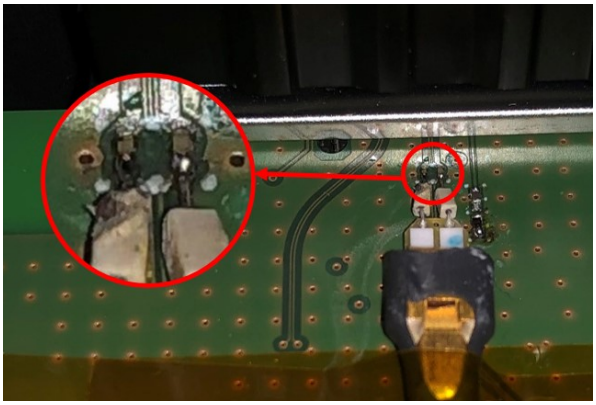


Figure 25. Differential probe tip.

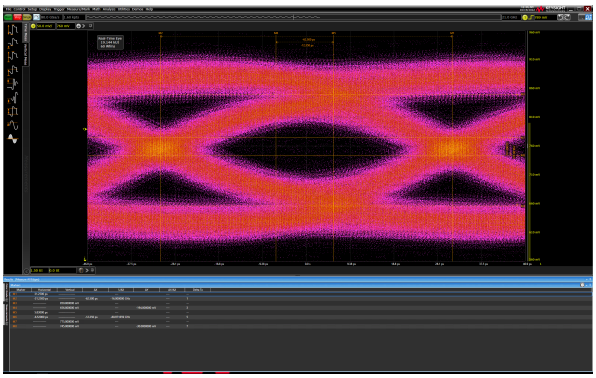


Figure 26. Eye pattern of a line without vias.

The actual measuring tip as shown in Figure 25 is soldered onto the plug-in card.

This is the best option without distorting the signal. The location was chosen so that the signal is detected as close to the receiver as possible. This is to capture as many of the effects of the routing as possible. Due to the equalization introduced in Chapter II-C3, it is not possible to measure the signal in the condition in which it later arrives at the receiver. For this purpose, the oscilloscope has a continuous time linear equalizer (CTLE) that reverses the influences of the link training and the signal is interpolated in such a way that it is most likely directed at the receiver.

IV. Evaluation of the Measurement Results

In this Chapter, the results of all measurements on the 10 designed plug-in cards are presented and discussed. For this purpose, the eye diagrams were measured with the oscilloscope presented in Chapter III-C for all cards and analyzed with regard to signal integrity.

A. No Via

Figure 26 shows the measured results of a PCIe lane.

This card was developed with full consideration of the PCIe specifications and serves as a reference for the

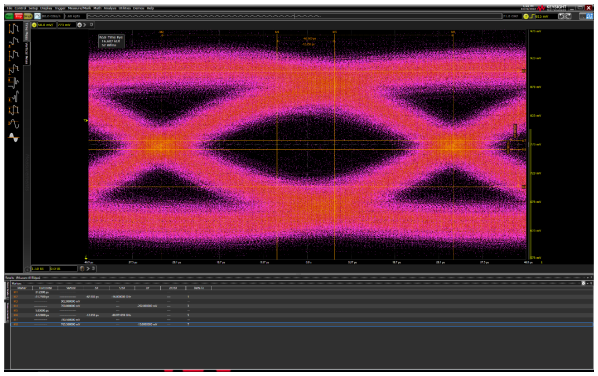


Figure 27. Eye pattern of lane 4.

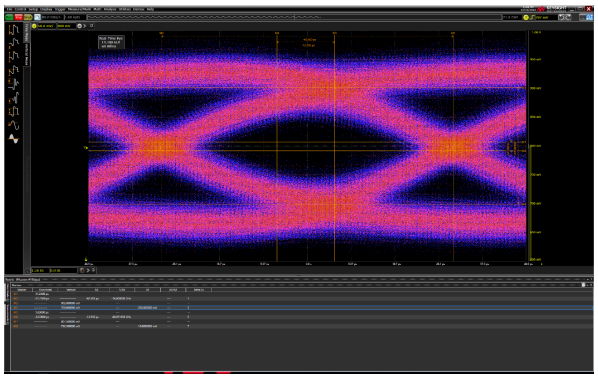


Figure 28. Eye pattern of lane 4.

following measurements. Peak-to-peak, the maximum signal level is about 300 mV. The eye height is about 90 mV. The crossing point is at 50% and the inside of the eye is a little noisy. The eye width is 36 ps and the mean UI center is in the middle of the eye. Apart from a few dots inside the eye, the mask is rarely violated, which indicates good signal integrity and corresponds to the result from the data throughput measurements.

B. Even Via (x4)

Figure 27 shows the measurement result of lane 4 which was modified to have 10 vias.

Peak-to-peak, the maximum signal level is about 350 mV, while the eye height is about 150 mV. The crossing point for this measurement is 50%. Horizontally, the eye width is about 37 ps and the mean UI center is right in the middle. The inside of the eye is a little noisier than in Figure 26, but the aperture is still easily recognizable, and the mask is rarely violated. In comparison to Chapter IV-A, it is noted that the amplitudes of this card are 1.3 dB higher. This is probably due to the link training, which is intended to compensate for the influence of the layer changes.

C. Odd Via

Figure 28 shows a measurement result of lane 4, but this time there is an odd number, 9, of vias.

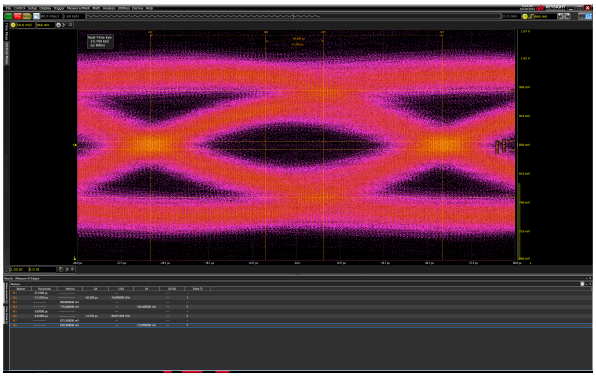


Figure 29. Eye pattern of a stripline with via stubs.

The maximum signal level is about 300 mV, while the eye height is about 110 mV. The crossing point is again at 50% and the center is exactly in the middle. At this lane, the eye width is about 40 ps, which is a bit wider compared to the two cards discussed above. The inside of the eye is only minimally noisy, and the mask is almost not violated at all. At first glance, this result does not match the performance in terms of data throughput, but it can be explained by the performance of the hard disk or the solder joints.

D. Microstripline

Figure 29 shows a measurement result of lane 1. In one section the line is routed as a stripline on an inner layer.

The maximum signal level is again around 300 mV and the eye height is 70 mV. Again, the crossing point is at 50%, and the UI center is in the middle. The eye width is about 32 ps. Looking at the eye, it is noted that it is much noisier in this measurement than in the previous measurements. This can be explained by reflections at the via stub. These seem to have a considerable effect on signal integrity.

E. Microstripline Microvia

Figure 30 shows the measurement result of lane 1 and, as in Chapter IV-D, the line is routed on a section as a stripline on an inner layer.

In this measurement, however, microvias without stubs were used instead of through-hole vias. This leads to a smaller maximum signal level, which is only about 250 mV here. The eye height, on the other hand, is considerably higher than in the previous measurement, at about 100 mV. The crossing point is at 50%, the center is in the middle and the eye width is 38 ps. This diagram exhibits almost no noise at all, and the mask is only very rarely violated. This demonstrates very clearly the difference of the via used. The signal level is -1.6 dB lower than with via stubs, which can be attributed to better signal integrity and adjusted link training.

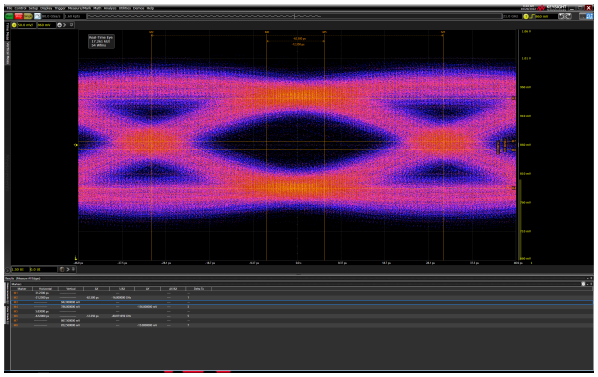


Figure 30. Eye pattern of a stripline without via stubs through the use of microvias.

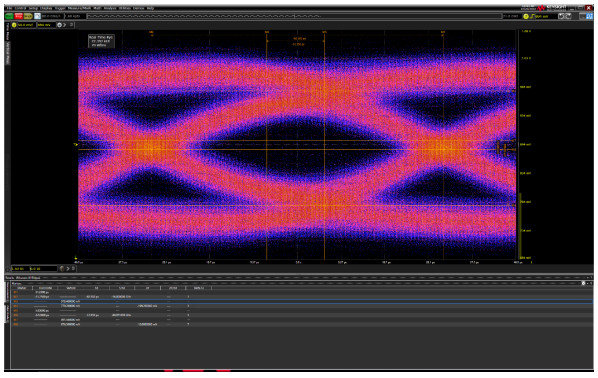


Figure 31. Eye pattern planecoupling without coupling capacitors.

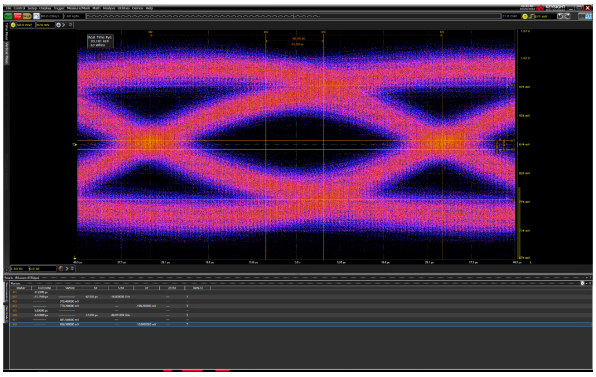


Figure 32. Eye pattern planecoupling with 2x 220nF coupling on each side.

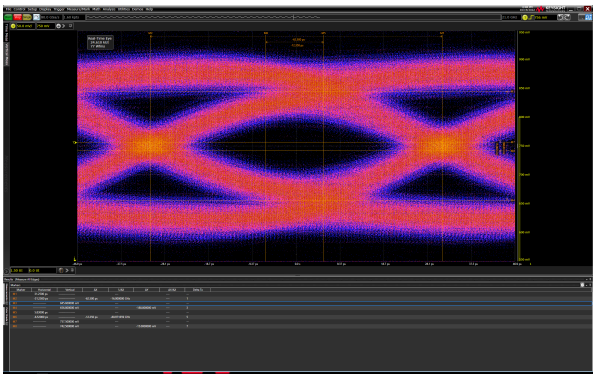


Figure 33. Eye pattern of a PCIe lane with one via.

F. Plane Coupling

Figure 31 shows the results of the first of two measurements on lane 1 where a line segment on the adjacent inner layer was coupled with a power delivery network (PDN). However, in the case shown here, the coupling capacitors are not populated.

The maximum signal level of this measurement is again about 300 mV. The eye height is about 100 mV and the crossing point is at 50%. The center is slightly to the right and the eye slightly resembles a diamond shape. The eye width is 38 ps. There is slight noise inside the eye, but the mask is barely violated.

In the results shown in Figure 32 the measurement was carried out again, now with equipped coupling capacitors.

With regard to the measurement results, hardly any differences from the pattern without coupling capacitors can be seen. Maximum signal level and eye height and width are similar to Figure 31. However, the eye is still a little bit less noisy.

G. Single Via

The measurement corresponding to the results shown in Figure 33 was carried out on lane 1.

The card is the same as the reference card, except for a layer change from top to bottom. The maximum signal level is again around 300 mV. The eye is a little narrower with a eye height of about 80 mV. The mean center is again in the middle of the eye and the crossing point is at 50%. The eye width is 38 ps. The eye interior shows little noise, and the mask is subject to little violation.

H. Single X-Via

Figure 34 shows a measurement result on lane 1 that is basically the same as the measurement result shown in Figure 33. However, here an "X-via" was used here to bend the lane at a 90-degree angle in the course of the layer change and to swap the polarity instead of routing a bend shape.

This modification has no effect on the maximum signal level. The eye width is slightly higher at about 100 mV. It is particularly noteworthy, however, that the inside of the eye is somewhat noisier compared to the results shown in Chapter IV-G.

I. Plane Coupling V2

This card featured several PDNs on the reference layer. Figure 35 shows the measurement results.

First of all, it is noted that the maximum signal level, which in all previous measurements on the cards discussed above had settled between 250 mV and 350 mV, is now close to 400 mV. The eye height is also

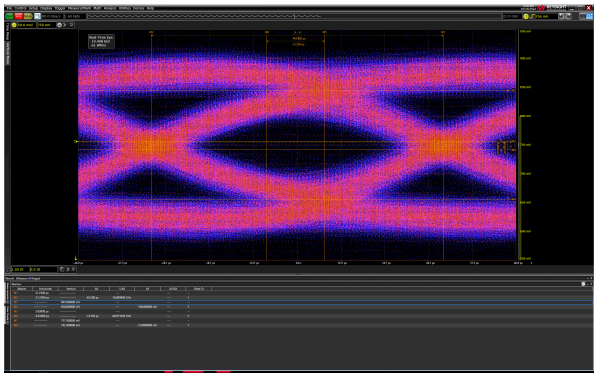


Figure 34. Eye pattern of a PCIe line with a 90° turn in a via.

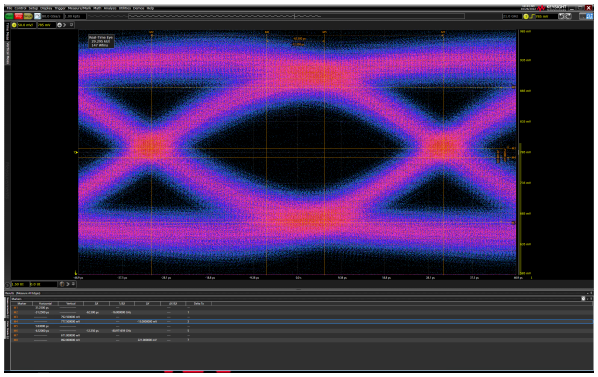


Figure 35. Eye pattern plane coupling V2 lane 4 uncoupled.

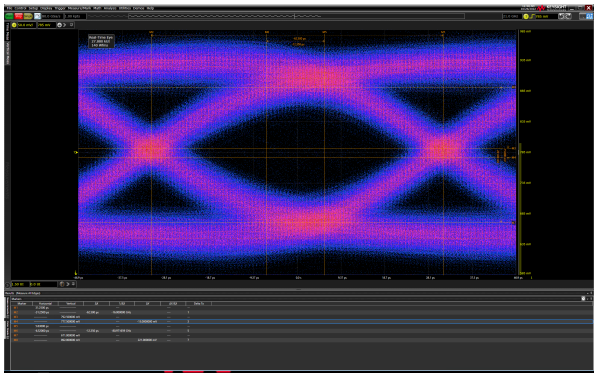


Figure 36. Eye pattern plane coupling V2 lane 4 coupled.

considerably higher than in the previous measurements, with a maximum opening of about 180 mV. The crossing point is at 50%, but the central UI center is shifted to the right and again resembles the diamond shape. The eye width is 42 ps. The eye is visibly noisy, even though the mask is found to be very clean in the eye. The higher voltage can be explained by a different preset in link training, which also automatically leads to steeper edges. The horizontal shift indicates inductive behavior, probably due to the disturbed return path.

Figure 36 shows results where the aforementioned PDNs were also connected to the ground reference via coupling capacitors in terms of wave properties.

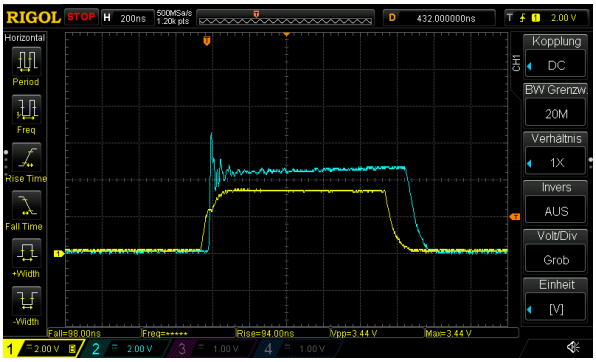


Figure 37. Signal of the noise source.

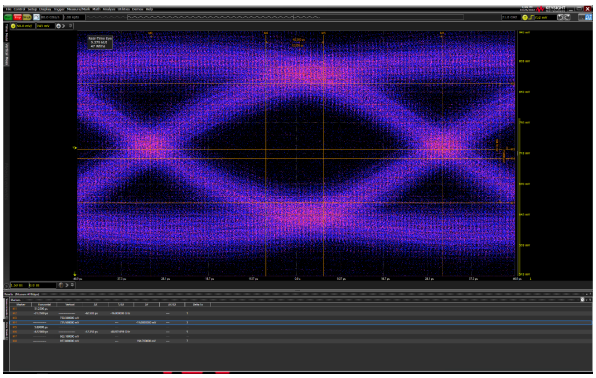


Figure 38. Eye pattern of a disturbed PCIe lane by EM-noise.

With regard to the maximum signal level and the eye height and width, there are no differences from the results shown in Figure 35. However, it is noted that the eye in this measurement is visibly less noisy than in the first measurement. In addition, the mask has moved a little closer to the center.

J. EME 500 kHz

In this test case, an electromagnetic emission (EME) interferer was installed on an internal layer during measurement, which is supposed to represent the use of neighboring circuit parts. Under certain circumstances, this can produce noise comparable to that of a real application. Figure 37 shows the characteristics of the noise source in blue while the corresponding control signal, which is generated by a frequency generator, is shown in yellow.

Figure 38 shows the eye diagram for the corresponding measurement.

Here, the maximum signal level is again relatively high at about $400\,\mathrm{mV}$. The eye height is about $150\,\mathrm{mV}$ and the eye width is $40\,\mathrm{ps}$. The crossing point is at $50\,\%$ and the center of the mask is in the middle. All the curves are highly diffused, and the eye is visibly noisy due to the interfering transmitter in this measurement. The mask is also frequently violated. This is consistent with the fact that data throughput

Table III
EYE CHARACTERISTICS AND RESULTS OF SPEED AND LINK STATUS

Board name	max. peak-to-peak signal level	eye height	crossing point	eye width	Payload bandwidth	Lane count	Link type
No via	300 mV	90 mV	50 %	36 ps	1.8 GB/s	×1	Gen 4
Even via (×4)	350 mV	150 mV	50 %	37 ps	6.5 GB/s	×4	Gen 4
Odd via (×4)	300 mV	110 mV	50 %	40 ps	5.9 GB/s	×4	Gen 4
Microstrip line	300 mV	70 mV	50 %	32 ps	1.8 GB/s	×1	Gen 4
Microstrip line Microvia	250 mV	100 mV	50 %	38 ps	1.8 GB/s	×1	Gen 4
Plane Coupling	300 mV	100 mV	50 %	38 ps	1.8 GB/s	×1	Gen 4
Single via	300 mV	80 mV	50 %	38 ps	1.8 GB/s	×1	Gen 4
Single X-via	300 mV	100 mV	50 %	38 ps	1.8 GB/s	×1	Gen 4
Plane Coupling V2	400 mV	180 mV	50 %	42 ps	5.2 GB/s	×4	Gen 4
EME	n.a.	n.a.	n.a.	n.a.	5.4 GB/s	×4	Gen 4
EME 500kHz	400 mV	150 mV	50 %	40 ps	4.8 GB/s	×4	Gen 4

is significantly reduced as soon as the source of interference is switched on.

K. Evaluation Summary

The measurement results of all 10 cards are summarized in Figure IV-J with respect to maximum peak-to-peak signal level, eye height, crossing point, eye width, payload bandwidth, lane count, and link type.

To classify the results: The theoretical maximum payload bandwidth of PCIe without protocol overhead is 1.97 GB/s on a single lane and 7.88 GB/s on four lanes.

As shown in Figure IV-J, all the plug-in cards worked with a Gen 4 link. The measured payload bandwidths for all plug-in cards with one lane are very close to the theoretical maximum. Only the plug-in cards with 4 lanes cause the measurement results to become scattered. If signal integrity declines and more faulty packets arrive at the receiver, the receiver notices this and requests them again. Since the information now has to be retransmitted, the effective data rate decreases. This may not necessarily be due to signal integrity issues, however, but might also be related to the maximum performance of the SSD hard drive.

V. CONCLUSION

The key question considered during this work was the effect of signal routing on signal integrity and thus payload bandwidth or data throughput. The PCBs developed for this investigation incorporate a wide range of different influences. These include various designs and numbers of vias, outer and inner layer behavior, wave impedance effects and, finally, provoked EM interference.

The physical fundamentals of data transmission were first addressed and related to an application, the PCIe bus. This is subject to very broad specifications when taking the principles of line theory into account. However, if the necessary knowledge is adapted, it provides an excellent working basis for a PCB developer. Through link training, the PCIe protocol is surprisingly well equipped and tolerant of minor layout errors. Nevertheless, the most important point is still that there must be enough space on the PCB for the individual lanes. The EME test has shown that neighboring circuit parts can have such a disruptive effect that significant performance losses occur, which are expressed metrologically by strong noise and a diffuse signal curve. Also, if the ground reference is changed several times, lower data rates have to be accepted. On a physical level, this is shown by more inductive behavior on the part of the data line. Layer changes are unproblematic, but attention must be paid to the choice of via used, as stubs have a negative effect on signal integrity.

The use of redrivers and retimers should be considered by the PCB designer, especially for longer lines or multiple connectors.

In terms of implementation it is easiest if data lines are routed on the outer layer, which is perfectly fine in terms of signal integrity. As expected, the stripline, with its internally routed lines, performs slightly better. On one hand, however, this does not help if interference signals are coupled in by high currents on adjacent layers. On the other hand, it can help with external radiation and long signal lines.

As robust as PCIe is, a good product does not stop at the board layout. The manufacturer should be consulted on the dimensioning of the tracks with regard to wave impedance, particularly in respect of the production of boards. It also makes sense to machine assemble the components as poor solder joints have a negative effect on overall stability and performance, and this may not necessarily be measurable.

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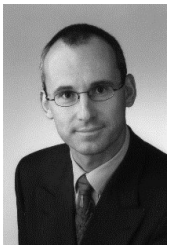

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